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Patent Application for

Radio Transmitter with Accurate Power Control

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Radio Transmitter with Accurate Power C ntrol

<u>Field of the Invention</u>

The invention generally relates to radio transmitters, and more specifically to accurate control of the broadcast power of radio transmitters.

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<u>Background Art</u>

Accurate control of the power transmitted by a radio is important for a variety of reasons:

• Regulatory bodies, such as the FCC, limit the maximum power of radio

10   transmissions.

• Transmitted output power level can have an uncertainty on the order of 10dB without closed loop control.

• Radio link range is a function of transmitted power such that higher power results in a link that can be maintained over a longer distance.

15   • Accurately controlling the transmitted power to the minimum needed to maintain a link minimizes interference with other radios and minimizes power dissipation.

Most radio transmitters use some form of closed-loop control as shown in Figure 1 to control output power. The transmitter is represented as a modulator

20   10, which outputs a modulated radio-frequency signal. The output of modulator 10 typically is amplified in multiple stages at least one of which is a variable-gain RF amplifier (VGA) 11, and another of which is a power amplifier (PA) 12. The output of PA 12 is then transmitted out antenna 13. A directional coupler 14 at the output of the PA 12 produces a power sensing signal that is proportional to the

25   power transmitted by antenna 13. The power sensing signal is detected by the

power detector **15** which produces a dc voltage proportional to the power

sensing signal at its input. The output of power detector **15** is input to a feedback

amplifier **16**, which controls the gain of the VGA **11** to minimize the difference

between the output of power detector **15** and a reference voltage input (Ref) to the

5   feedback amplifier **16**. The circuit shown in Fig. 1 may be part of a half-duplex

transceiver in which the transmitter and the receiver alternately cycle such that

they are not both on at the same time.

        Power detector **15** is typically either a diode detector or a logarithmic

amplifier. Diode detectors are inexpensive, but they have limited dynamic range

10   (~ 20dB) and suffer from temperature dependence. Logarithmic amplifiers can be

very accurate, but their frequency range is limited. Present state-of-the-art

logarithmic power detectors have a maximum frequency on the order of 2.5GHz.

That frequency can be increased, but only at the expense of increased power

dissipation.

15   In addition, the analog closed-loop system shown in Figure 1 is more

complicated if the rf output from modulator **10** includes a varying modulation

envelope, since the loop will attempt to regulate away the varying envelope. This

effect can be addressed by using a partly digital loop which digitizes the output of

power detector **15**.

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Summary of the Invention

        A representative embodiment of the present invention includes a radio

transmission power control circuit in which a radio frequency (rf) downconverter

that produces a downconverter output having a frequency equal to the frequency

25   difference between a first downconverter input based on a transmitted signal of a

radio transmitter and a second downconverter input based on a local oscillator

signal. A receiver baseband circuit processes the downconverter output to

produce a power signal representative of the transmitted signal. A feedback control circuit produces a transmitter gain control signal to control transmitted signal power so as to minimize the difference between the power signal and a power reference signal.

5   In a further embodiment, the circuit is part of a half-duplex radio transceiver also having a receiver circuit such that the receiver baseband circuit is used by the receiver when the radio transmitter is inactive, and wherein the local oscillator signal is used by the radio transmitter such that the transmitted signal has a frequency determined by the local oscillator signal.

10   An embodiment may also include an analog to digital converter that converts the power signal to a representative digital power signal such that the feedback control circuit produces the transmitter gain control signal so as to minimize the difference between the digital power signal and the power reference signal.

15   In other embodiments, the first downconverter input may be developed by a directional coupler that senses the transmitted signal. The radio transmitter may be part of a wireless local area network transceiver. In addition or alternatively, the radio transmitter may be part of a time division duplex system.

            Embodiments of the present invention also include a method of controlling
20   radio transmission power. A radio frequency (rf) downconverter output is produced having a frequency equal to the frequency difference between a first downconverter input based on a transmitted signal of a radio transmitter and a second downconverter input based on a local oscillator signal. The downconverter output is processed with a receiver baseband circuit to produce a
25   power signal representative of the transmitted signal. A transmitter gain control signal is produced to control transmitted signal power so as to minimize the difference between the power signal and a power reference signal.

The radio transmitter may be part of a half-duplex radio transceiver also having a receiver circuit such that the receiver baseband circuit is used by the receiver circuit when the radio transmitter is inactive, and the local oscillator signal may be used by the radio transmitter such that the transmitted signal has a

5   frequency determined by the local oscillator signal.

A method may further include converting the power signal to a representative digital power signal such that the transmitter gain control signal is produced so as to minimize the difference between the digital power signal and the power reference signal.

10   In any such a method, the first downconverter input may be developed by a directional coupler that senses the transmitted signal. The radio transmitter may be part of a wireless local area network transceiver and/or a time division duplex system.

15   Brief Description of the Drawings

The present invention will be more readily understood by reference to the following detailed description taken with the accompanying drawings, in which:

Figure 1 shows a typical radio frequency transmitter having closed loop feedback control.

20   Figure 2 shows functional blocks of a radio system according to one embodiment of the present invention.

Figure 3 shows a high-level functional block diagram of one specific embodiment of the control loop gain control and control blocks.

Figure 4 shows functional blocks within the power control loop structure of

25   Fig. 3.

Figure 5 shows the relative timing of some of the signals associated with the transmit power control of Fig.5.

Figure 6 shows a plot of signal-to-noise ratio of the detected power and detector path gain in comparison to output power for one embodiment.

Figure 7 shows output power and desired power versus transmit burst number in one embodiment.

Figure 8 shows a histogram of output power in an embodiment with 0.25 dB rssi resolution and 0.125 dB gain steps.

Detailed Description of Specific Embodiments

Embodiments of the present invention are directed to techniques for accurate control of radio transmitter power. Some radio systems, for example time-division duplex (TDD) systems such as 802.11(a)(b)(g) wireless local area networks (WLAN's), use the same frequency for transmitting and receiving. In such systems, the receiver and the transmitter cannot be used at the same time. Embodiments of the present invention provide very accurate control of the transmitted power by utilizing the receiver base-band section, which is idle while transmitting, together with an RF downconverter with very accurate gain and a digital control block. Such an approach offers far more accurate power level control at lower cost. This results in increased range in the radio link, or lower power dissipation, or both.

In the specific instance of an 802.11(a)(b)(g) WLAN, the a-band frequency range of 4.9 to 5.9GHz is too high for a practical logarithmic amplifier. And the power control range of 45dB is too large for a diode detector. Because the 802.11 standard is a time-division duplex (TDD) system, the receiver and transmitter – which use the same frequency channel – are not used at the same time. Thus, a direct-conversion transmitter in which the transmit local oscillator (LO) is at the carrier frequency can use the receiver's baseband path during the transmit cycle.

Figure 2 shows a block diagram of a radio system according to one

embodiment of the present invention. As before, modulator 10 outputs a modulated rf signal, in this case, to a two-stage variable gain amplifier (VGA) 11. The output of VGA 11 is provided via transmit bandpass filter 21 to power amplifier (PA) 12, and from there via transmit output filter 22 out the antenna 13.

5   The transmitted rf output power is detected by a directional coupler 14, which drives a power detect downconverter stage comprised of a downconverter input amplifier 23 and power detect downconverter 24. In principle, the downconverter of the receiver could be used, but in practice it is not desirable to do so because the requirements for the receiver – low noise, high linearity and

10   high gain – are not compatible with the requirements for the power detector which are temperature- and frequency-independent gain. It may be noted that the area of a modern RF IC tends to be dominated by inductors. Compared to the areas of the receiver and transmitter circuits, the area of the power detector downconverter stage is negligible.

15   The output of the power detect downconverter 24 is fed to one of the receiver's baseband paths where it is filtered by baseband filter 25 and amplified by baseband VGA 26 The output of baseband VGA 26 is digitized by control loop ADC 27. The digital output of ADC 27 is provided to control block 28, which together with gain control 20 generates a control signal for the transmitter VGA's

20   11 so as to minimize the difference between the digital power detect signal from the control loop ADC 27 and a reference cal signal input to control block 28.

The power detect signal from the directional coupler 14 to the downconverter input amplifier 23 is relatively large, on the order of –15dBm in one specific implementation at maximum output power, so the downconverter

25   stage does not need gain. In one specific embodiment, the gain of the downconverter input amplifier 24 is –6dB, and the conversion gain of the downconverter 23 is –10dB. Since the downconverter input amplifier 23 can have

loss, a resistive load may be used with a very small resistance such that the bandwidth is very wide. This approach means that frequency dependence of the downconverter stage is very small even at very high frequency. In addition, resistively loaded circuits can be designed with a gain that is a function of the ratio of two resistors. The result is very predictable and constant gain which minimizes or even eliminates calibration requirements.

In one specific embodiment, the downconverter 24 has a transconductance of 3.2 milliSiemens, which results in a maximum gain of 19.7dB when loaded by the variable transimpedance baseband VGA 26. The receiver baseband gain should be set so that the control loop ADC 27 does not clip under maximum input-level conditions and so that adequate signal-to-noise ratio (SNR) is maintained over all of the transmit output power range. The maximum input level at the input to the downconverter input amplifier 23 is designed to be –15dBm. An additional 16dB of headroom is added (10dB for the peak-to-average, 3dB for uncertainty in the detector path gain and another 3dB for uncertainty in the coupler loss). Thus, the receiver baseband gain is set so that the input to control loop ADC 27 is 16dB below the clipping level with a -15dBm input power. This condition is met with the receiver baseband gain set to –9dB. Operation gets close to the desired gain at about 30dB below maximum gain.

As the output power is decreased, the SNR of the detected power is decreased as well. To ensure an accurate measure of transmitted power, SNR should be kept above about 20dB nominally. A plot of SNR and detector-path gain versus output power for one specific embodiment is shown in Figure 6. For every 15dB of output power reduction the receiver baseband gain is increased by 15dB in order to maintain adequate SNR. In order to implement the gain control as shown in Figure 6, the power control loop needs to control receiver baseband gain during a transmit burst. Calculations for one specific embodiment suggest

that the optimum initial setting for the receiver baseband gain is 30dB below the maximum. It may be desirable to have the initial receiver baseband transmit burst gain setting be a variable that is written to a circuit register upon system power up.

5   As described above, the gain control 20 determines the transmit output power level. The gain control 20 can set the transmit power as close to the desired output power as possible without going over. Transmitting at the highest output power that does not exceed FCC limits maximizes link range. The power detect control loop that the gain control 20 is a part of should converge to the final

10   output power as quickly as possible. In one specific embodiment, convergence within two transmit bursts can be achieved. After the second transmit burst, it is possible to change the transmit power level with very high accuracy.

A high-level functional block diagram of one specific embodiment of the control loop gain control 20 and control block 28 is shown in Figure 3. Control

15   block 28 represents some combination of software and hardware that is used to control the radio.

Control block 28 receives reference input signals TxCal and PDCal. Transmit reference signal TxCal is a 7-bit constant that is used to calibrate the transmitter's gain. In one specific embodiment, the least significant bit (LSB) of TxCal may be

20   0.25dB, and the range may be 32dB. The power detect reference signal PDCal is a 8-bit constant that is used to calibrate the power detector. In one specific embodiment the LSB of PDCal may be 0.25dB, and the range may be 64dB. Different TxCal and PDCal words may be needed for each different transmission frequency band. For example, different TxCal and PDCal words may be used for

25   ISM band and for UNII band. These constants may be stored in memory such as flash memory and loaded when the system is started up.

The TxAtten output from control block 28 to gain control 20 represents the

desired amount of attenuation requested. For example, if the maximum output power allowed in a certain band is requested, TxAtten will be 0dB. In one specific embodiment, the output power is programmable over a 56.5dB range with 0.5dB resolution so TxAtten is a 7-bit word. Control block 28 also outputs to

5 gain control 20 a power control loop reference pdref, which is typically an 8-bit word (LSB=0.25dB) that is a function of PDCal and TxAtten. The received signal strength indicator signal rssi is typically a 8-bit (LSB=0.25dB) measure of the transmitted power. The power control loop generally, and gain control 20 specifically, minimize the difference between pdref and rssi.

10 The gain control 20 is initialized by the reset signal, reset. The power detect enable signal, pdet, enables the power detect circuit within the gain control 20. Transmit enable signal, Tx, enables the transmitter and clocks the gain control circuit 20.

Gain control 20 produces two outputs, Atten and Rx_gain. Atten is the

15 transmit path attenuation that is set by the power control loop, *i.e.*, the gain control for transmit VGA 11. For example, in one specific embodiment, Atten is a 10-bit word in which the LSB is 0.138dB. Rx_gain is the receive-path gain signal which is used to optimize the gain of baseband VGA 26 to maximize the signal-to-noise ratio (SNR) of the detector path while preventing the control loop ADC 27

20 from clipping.

In some embodiments, a factory calibration may be required for the power control loop. The calibration can be performed by transmitting a signal – either the OFDM preamble or a single tone – and measuring the power. The transmit reference TxCal is determined by:

25 $$TxCal = P_{cal} - P_{desired} - FudgeFactor$$

where P_{cal} is the measured power and $P_{desired}$ is the desired power. The *FudgeFactor* ensures that the output power of the first burst does not exceed the FCC limit

because the frequency and temperature used during calibration mode may not

result in the highest possible output power. The power detect reference PDCal is

determined by:

$$PDCal = rssi_{cal} - P_{desired} + P_{cal}$$

5   where $rssi_{cal}$ is the rssi reading during the calibration test. It may be desirable to

perform the calibration at something other than 0dB attenuation to ensure that the

transmit path is linear. In that case, TxAtten should be added to PDCal. This can

be done in the test software.

Figure 4 shows functional blocks within the power control loop structure of

10   Fig. 3. Initially, we ignore the path along the top and determine the attenuation

output from the gain control 20, Atten, during burst number n as:

$$Atten(n) = Atten(n-1) + rssi((n-1) - pdref$$
$$= Atten(n-1) + rssi(n-1) - PDCal + TxAtten$$

where pdref is the power control loop reference, which is the target rssi adjusted

for the desired attenuation setting. For example, if the transmit power during

15   burst n-1 is 2dB too low, rssi(n-1)-pdref = -2dB, so the Atten signal for burst n will

be reduced by 2dB. If the attenuation steps for Atten are accurate, the power level

will get to the desired level (within the quantization error) on the second transmit

burst.

It is possible for the desired transmit power to change from one burst to the

20   next. Once the loop has stabilized (*i.e.*, after the first burst) the transmitter will

transmit at the correct power – even if the desired power level changes – because

pdref changes if TxAtten changes. For example, if TxAtten was 0dB but is

changed to 3dB after the end of a transmit burst, then pdref will fall by 3dB so

rssi-pdref will be 3dB and the attenuation will increase by 3dB.

25   The attenuation setting Atten for the first transmit burst (TxAtten0) is

calculated differently than for subsequent bursts because there is no previous

burst that can be used to measure the error. Thus, as shown along the top row of Fig. 4, the first-burst attenuation setting is TxAtten+TxCal. The multiplexer MUX at the output of gain control 20 selects between the open-loop calculation of the attenuation for the first burst and the closed-loop control for subsequent bursts. In

5   one specific embodiment, adders A1, A2 and A2 are 8-bits wide, and A4 is a 10-bit adder.

The timing of some of the control signals for the transmit power control in Fig. 4 are shown in Figure 5. The load synthesizer signal *reset* is asserted when a new frequency channel is selected. The first burst on the new channel will use the

10   *Tx* attenuation setting calculated by the feedforward path and selected by *mux_sel* going low. *mux_sel* goes high on the first falling edge of *Tx* after the rising edge of *reset*. When *mux_sel* is high the closed-loop power control is selected. *pdet* enables the power detect circuits and one of the receiver baseband channels. *pdet* only has to be asserted long enough to get a stable *rssi* reading. In one specific

15   embodiment, it may take about 1μsec for the *rssi* averaging to settle, and another 1 μsec for the receiver filter to settle.

The basic approach described above can be verified by a simple matlab program. Figure 7 shows the output power and the desired power versus the transmit burst number. A histogram of the output power in an embodiment with

20   0.25dB rssi resolution and 0.125dB gain steps is shown in Figure 8. The desired power is 16dBm for the first 5 bursts and 10dBm for next 5 bursts. There is a significant error during the first burst since the calibration cannot account for temperature and frequency dependence. After the first burst the error is very small (limited by gain and rssi quantization) even if the desired output power

25   changes.

The following table provides a block specification of the transmit power control function for one specific embodiment:

Pin Name	I/O	Description
vdd18	S	1.8V supply
vss	S	ground and local Nwell
substrate (global)	S	substrate
tx_atten[6:0]	I	desired attenuation. LSB=0.5dB
txcal_lb[6:0]	I	low-band tx power calibration word. Written to SIF on power up. LSB=0.25dB.
txcal_hb[6:0]	I	high-band tx power calibration word. Written to SIF on power up. LSB=0.25dB
pdcal_lb[7:0]	I	low-band rssi calibration word. Written to SIF on power up. LSB=0.25dB
pdcal_hb[7:0]	I	high-band rssi calibration word. Written to SIF on power up. LSB=0.25dB
Rssi[7:0]	I	digital rssi output. LSB=0.25dB. Rx AGC uses rssi[9:2].
reset	I	loads new synthesizer word and resets the power-control loop. first burst after rising edge of ld_synth uses feedforward path.
Tx	I	enables transmitter. atten is latched on rising edge of tx.
pdet	I	enables the power detector circuits and one of the RxBB paths. rssi output is latched on falling edge
atten[9:0]	O	Tx attenuation. 30dB in the upconverter (2, 3dB steps followed by 4 6dB steps). 27dB in 3dB steps in the mixer. 2.875dB in 0.125dB steps in the digital multiplier preceding the DAC.
rx_init_gain[4:0]	I	Rx-gain setting when tx_atten_in[6:0]=0dB. Written to an AFE register upon power up.
rx_gain[4:0]	0	Rx VGA gain setting. Equal to rx_init_gain for −15dB < tx_atten < 0, rx_init_gain +15dB for −30 < tx_atten < -16, rx_init_gain + 30 dB for −45 < tx_atten < -31.

Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention.